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# Robustness of SiC MOSFETs in short-circuit mode

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The Power Point Presentation will be available after the conference.

## Abstract

This paper presents experimental robustness tests of Silicon Carbide (SiC) MOSFETs submitted to short-circuit operations. MOSFETs manufactured from different manufacturers have been tested and show different failure modes. A gate leakage current is detected before failure but is not necessarily responsible for the failure. For some tested devices, the failure appears in an open state mode after physical short-circuit between gate and source. The main failure mode is nevertheless a physical short-circuit between drain and source. However, the various tests show, despite the gate leakage current, excellent robustness of the various tested SiC MOSFETs under short-circuit.

## 1. Introduction

Various scientific literatures reported the excellent switching performances of silicon carbide (SiC) power MOSFETs in large market applications [1],[2]. From an industrial point of view, aside from switching performances, the robustness is also a major feature which has to be considered for power conversion systems [3]. Apparently, SiC MOSFETs, as new generation of power devices, are expected to offer superior robustness under extreme operation conditions, particularly in short-circuit (SC) operation compared to Si devices.

By comparison to Si ones, SiC MOSFETs possess smaller oxide thickness, coupled with a higher electric field for a given gate bias. This makes these devices sensitive to electron tunneling into and through gate oxide [4],[5]. Tunneling current is one of the main degradation mechanisms on gate oxide layer to SiC power MOSFETs [5]. SC with high current density and high temperature in the channel may increase the tunneling effect. So, it is of the first importance to carry out studies on the SC capability of SiC MOSFETs.

In this paper, short circuit tests are achieved on two types of 1200 V SiC MOSFETs manufactured by Cree (CMF20120 and C2M0080120) and a third type of MOSFETs from Rohm (SCT2080KE), as shown in Table 1. Destructive tests are carried out in order to analyze the behavior of the different SiC MOSFETs under SC but also analyze the mechanisms of failure.

Power device	$V_{BR}$ (V)	$I_{D(max)}$ (A)	$R_{DS(on)}$ (m $\Omega$ )
A- MOSFET	1200	42.0	80
B- MOSFET	1200	31.6	80
C- MOSFET	1200	40.0	80

Table 1. Electrical characteristics of tested power SiC devices

## 2. Experimental set-up

Fig. 1 shows the schematic of the experimental setup proposed to perform the short circuit tests for MOSFETs. A 6.5 kV IGBT mounted into the test bench is used to keep the device under test (DUT) from further damage after short-circuit failure. A positive voltage of +18V delivered by the driver allows to turn on the DUT via a gate driver resistance  $R_G$ . A negative voltage of -5 V is applied to the gate to keep them off.

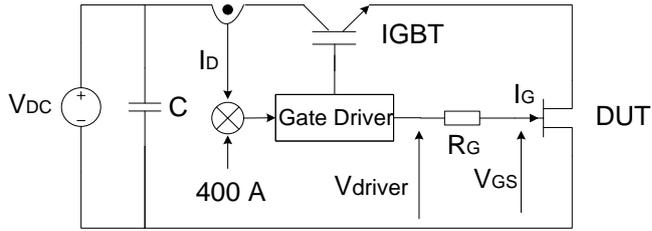


Fig. 1 Schematic of short-circuit test circuit for MOSFET.

Critical energy  $E_C$ , which is an essential feature of robustness to power device, refers to the minimal dissipated energy that leads to the failure of the tested device after one short-circuit. With the purpose of estimation of critical energy, the short-circuit duration is regularly increased from a low value (where the device is able to turn-off the SC current) up to the failure appears. The maximum energy the device is able to sustain during a safe short-circuit test is recorded as critical energy.

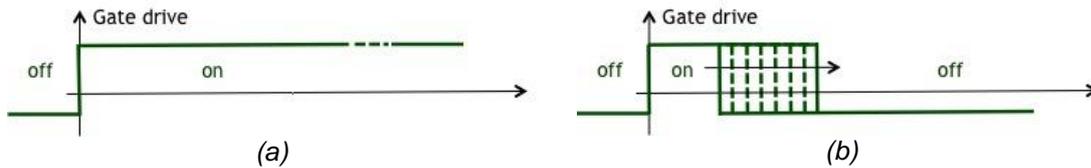


Fig. 2 Robustness tests under (a) current limitation and (b) short-circuit.

The paper will analyze for different case temperatures (from  $25^\circ\text{C}$  up to  $150^\circ\text{C}$ ) the robustness of the different SiC MOSFETs under current limitation mode when the device is maintained in the on-state until failure and under SC circuits with increased SC duration until failure. Meanwhile, influence of gate driver resistor and of temperature on short circuit failure will be investigated.

### 3. Robustness in current limitation mode

#### 3.1. Experimental results

A first batch of destructive tests are performed with a bus voltage  $V_{DC}$  of  $600\text{ V}$  for case temperature  $T_{case} = 25^\circ\text{C}$ . The duration of short circuit  $t_{S,C}$  is set up long-enough ( $80\ \mu\text{s}$ ) to ensure the presence of failure under every single short circuit test.

The commutation of drain-source voltage  $V_{DS}$  and drain current  $I_D$  of A-MOSFET are shown in Fig. 3. (a). Initially, drain current increases rapidly and reaches the saturation level. After a peak of drain current, a significant decrease to about  $100\text{ A}$  after about  $15\ \mu\text{s}$  of SC is noticed due to the reduction in carrier mobility with temperature growth [6]. This process is related to self-heating within DUT under such a severe operation. In addition, gate voltage  $V_{GS}$  falls gradually from  $10\ \mu\text{s}$  to the occurrence of failure as shown in Fig. 3(b). The decrease of  $V_{GS}$  is due to a gate leakage current measured during the tests. This particular behavior has already been shown on other SiC MOSFETs in [7]. The origin of the leakage current increase has been explained by tunneling effect mentioned above in [5]. Maximum gate leakage current is about  $50\text{ mA}$  for A-MOSFET and  $100\text{ mA}$  for B-MOSFET. In these current limitation operations, failure appears with a simultaneous short-circuit between the three terminals of the samples. The dissipated energy responsible for the failure of A-MOSFET is equal to  $1.12\text{ J}$  and  $0.714\text{ J}$  for B-MOSFET. Fig. 4 depicts similar transient to A-MOSFET with an earlier fault event. In this case gate voltage reduction appears after  $5\ \mu\text{s}$  and becomes more significant for B-MOSFET compared to A-MOSFET due to a higher gate leakage current.

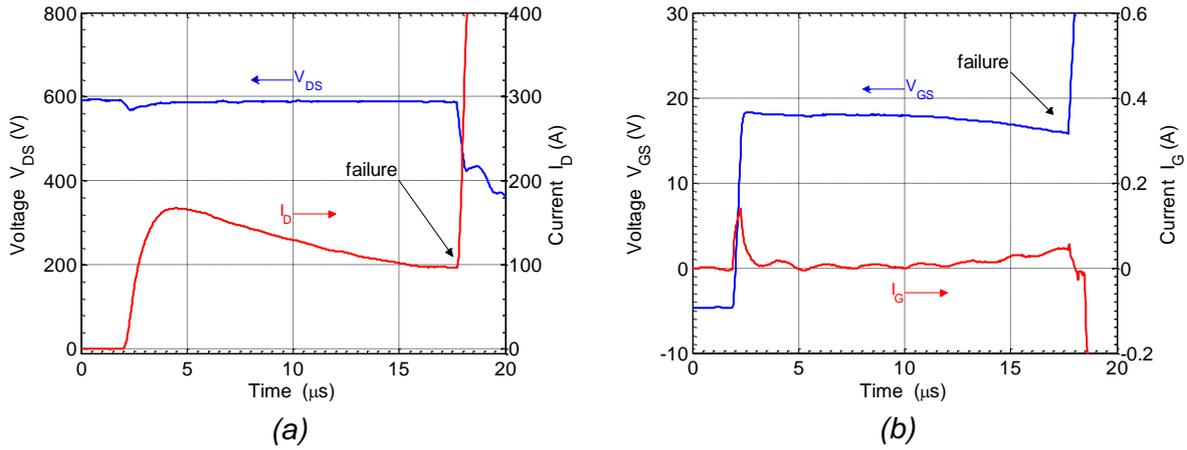


Fig. 3. Destructive test of A-MOSFET. (a) Drain and (b) gate waveforms, for  $R_G = 47 \Omega$ ,  $T = 25^\circ\text{C}$ .

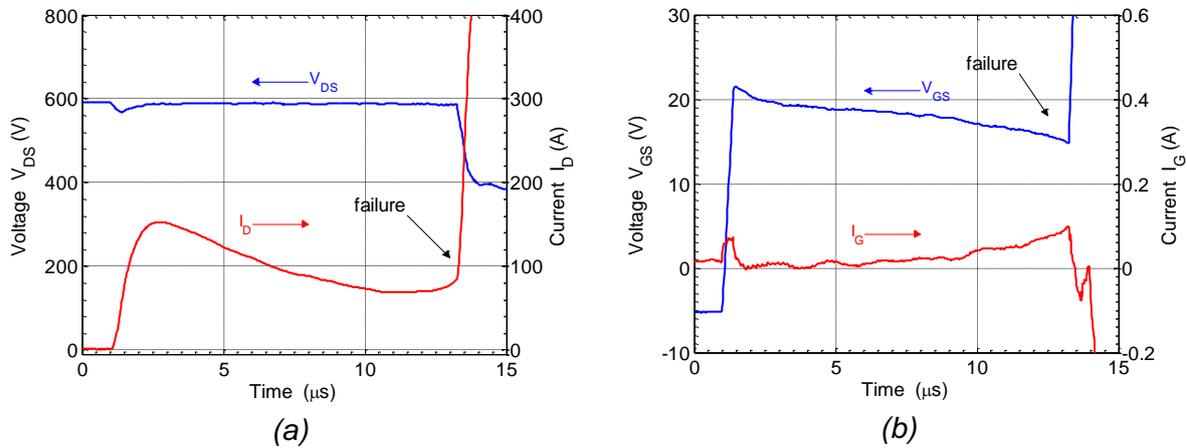


Fig. 4. Destructive test of B-MOSFET. (a) drain and (b) gate waveforms, for  $R_G = 47 \Omega$ ,  $T = 25^\circ\text{C}$ .

Under same experimental conditions, C-MOSFET's behavior differs from A and B-MOSFETs. It can be observed a prior failure of the gate oxide after  $19 \mu\text{s}$  (Fig. 5. (b)). The failure of the oxide results in a short circuit between gate and source and explains the gate current limited to  $0.37\text{A}$  by the driver resistor. Moreover, it seems that the failure between gate and source allows to switch off the drain current and to protect the device from destruction between drain and source as shown in Fig. 5 (a). In fact, drain-to-source voltage remains keeping  $+600 \text{ V}$  after failure of the oxide. This particular mode of failure is very interesting because of the off-state behavior between drain and source after failure between gate and source. The dissipated energy responsible for the gate oxide failure after  $19 \mu\text{s}$  is about  $1.57 \text{ J}$  in these conditions of operation.

In Fig. 6, for another tested C-MOSFET, after the oxide failure and the suppression of the channel, the remaining drain leakage current is high enough to be responsible for a thermal runaway and, in this case a dramatic failure appears between drain and source. Excessive power dissipation produced by drain leakage current after the oxide failure explains the thermal runaway and the ultimate failure of the device. The thermal energy dissipated before the occurrence of first failure on the oxide is about  $1.71 \text{ J}$ . In the two above short circuit tests on C-MOSFETs, even through the quantities of thermal energy leading to failure between gate and source are quite closed, the appearance of drain-source delayed failure clearly depends on the level of the remaining drain leakage current which is probably due to the temperature inside the device after oxide failure.

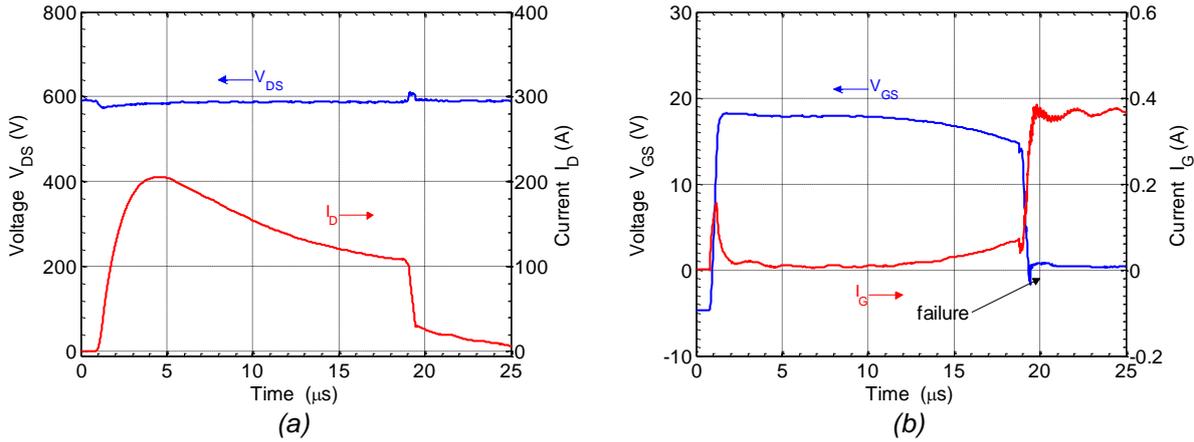


Fig. 5. Destructive test of C-MOSFET#1. (a) drain and (b) gate waveforms,  $R_G = 47 \Omega$ ,  $T = 25^\circ\text{C}$ .

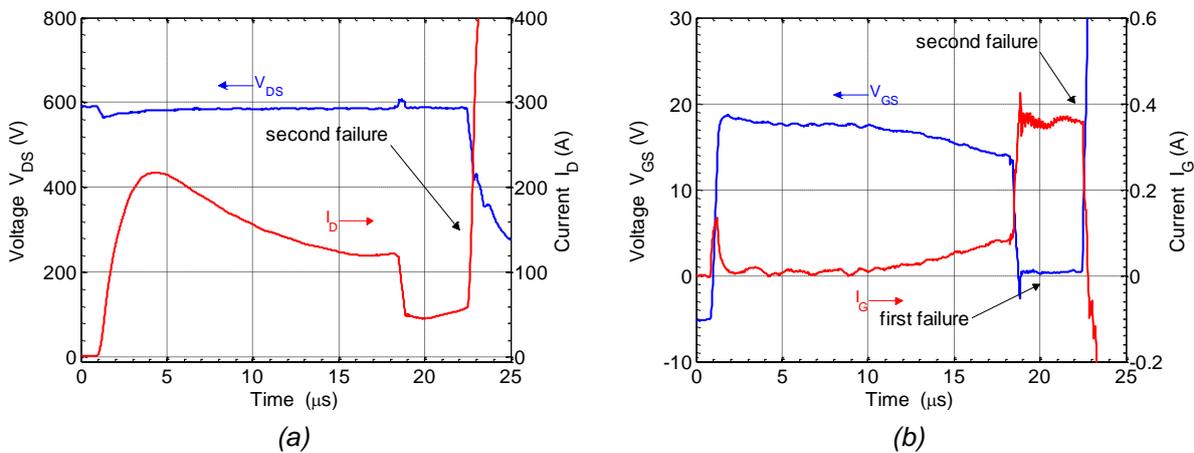


Fig. 6. Failure during SC of C-MOSFET#2. (a) drain and (b) gate waveforms,  $R_G = 47 \Omega$ ,  $T = 25^\circ\text{C}$ .

### 3.2 Discussions

Gate waveforms of all tested MOSFETs display reduction in gate voltage before failure, leading to the gate degradation, especially in gate oxide, which could be interpreted by a remarkable increase in the gate leakage current as shown on the different experimental results shown before. The presented results clearly show the tunneling effect, but it is not yet possible, at this stage of the study, to correlate the increase of the tunnel current to the failure. It is nevertheless important to note that the robustness of SiC MOSFETs is very comparable to those of Si MOSFETs instead of the fragility of the oxide during these very constraining modes of operation.

All of the failures can be classified by failure location on power MOSFETs into two categories. First, for A and B MOSFETs, failures occur on both gate and drain terminals. Similar results on SiC MOSFETs and JFETs has been observed in [10–12]. Due to high temperature reached by the device, the surface metallization is melted and can results from a local fusion of the device. Furthermore, a numerical thermal dynamic simulation reported in [10] confirms beyond the fusion limit of metallization, over-high temperature is responsible for this kind of failure.

In the second category, the failure first appears between gate and source after increase of the leakage gate current. The failure with a short circuit between gate and source nevertheless allows switching off the drain current after gate driver becomes uncontrollable. For one of the tested devices, a fail-safe failure is observed between drain and source. We also observed on one of the tested device a delayed failure between drain and source after failure at the level of the gate or the oxide. Because of high junction temperature, activation

of the parasitic bipolar junction transistor can be considered to explain the significant current flow from drain to source, which leads to an uncontrolled increase of the drain leakage current (thermal runaway).

Table 2 summarizes the experimental results for these different tests on SiC MOSFETs.

MOSFET	$t_{fail}$ ( $\mu$ s)	$E_{SC}$ (mJ)	Mode of failure
A	16.0	1118	(SC <sub>GS</sub> ) and (SC <sub>DS</sub> )
B	12.5	714	(SC <sub>GS</sub> ) and (SC <sub>DS</sub> )
C #1	18.0	1567	(SC <sub>GS</sub> )
C #2	17.5	1582	(SC <sub>GS</sub> ), then (SC <sub>DS</sub> )

Table 2 Summary of S.C tests on A, B and C MOSFETS

Where  $t_{fail}$  is the failure time,  $E_{SC}$  is the dissipated energy leading to failure, (SC<sub>GS</sub>) refers to short-circuit between gate and source, (SC<sub>DS</sub>) refers to short-circuit between drain and source.

#### 4. Short circuit robustness & Critical energy estimation

A series of non-destructive short circuit tests are carried out for the purpose of critical energy evaluation. The tests are performed at +600 V bus voltage and 150°C as initial test temperature with gate resistor  $R_G = 10 \Omega$ . For A and C- MOSFET the critical energy is estimated by successive short circuit tests with  $t_{sc}$  increasing by 1  $\mu$ s at each test until MOSFET failed.

The first results on A-MOSFET are plotted in Fig. 7, where drain-to-source and gate-to-source voltages are presented on the left scale and gate voltage is multiplied by 20 to match drain voltage scale. For test duration of 10  $\mu$ s and 11  $\mu$ s, after A-MOSFET turns off, current returns to zero. For test duration equal to 12  $\mu$ s the gate to source voltage controls the drain current, but few  $\mu$ s after the drain current switch off, failure appears with a short-circuit between the three terminals of the device. The estimated critical energy is about 852 mJ corresponding to 11  $\mu$ s, whereas this device failed for duration  $t_{sc} = 12 \mu$ s, which is similar to failure of B-MOSFET.

A sample of C-MOSFET does not present a failure until duration reaching to 12  $\mu$ s as well as A-MOSFET (Fig. 8). However its critical energy is about 1.06 J for duration of 11  $\mu$ s, 24% higher than that of A-MOSFET. Due to gate failure, gate and source terminals were shorted 11  $\mu$ s after turning-off. On the other hand, drain voltage still takes +600V and drain current is maintained to zero, which indicates the drain electrode works well. In these conditions, the failure in the gate oxide or between gate and source appears with a short circuit between gate and source which allow maintaining an off-state between drain and source. This particular mode of failure is very interesting for power electronics applications. If this mode of failure is reproducible it will confer a more favorable robustness of C-MOSFET especially for high temperature application.

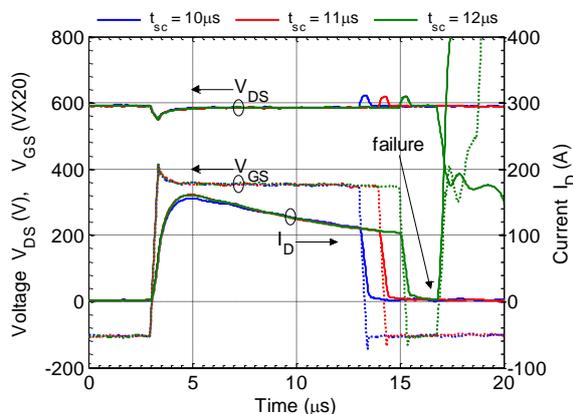


Fig. 7. Short circuit behavior of A-MOSFET for  $R_G = 10 \Omega$  and  $T_{CASE} = 150^\circ\text{C}$ .

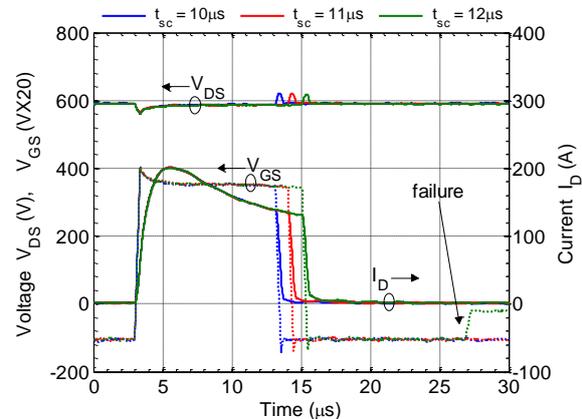


Fig. 8. Short circuit behavior of C-MOSFET for  $R_G = 10 \Omega$  and  $T_{CASE} = 150^\circ\text{C}$ .

## 5. Effect of case temperature and gate driver resistor

### 5.1. Effect of case temperature

These following tests are aiming at the affection of case temperature on short circuit capacity of SiC MOSFETs. The experimental conditions (current limitation) applied to MOSFETs are defined by: bus voltage = +600 V and SC duration = 80  $\mu$ s.

Fig. 9 (a) and (b) show the waveforms measured on A-MOSFET under destructive short circuit stress with  $R_G = 10 \Omega$  for  $T_{CASE} = 25^\circ\text{C}$  and  $150^\circ\text{C}$ . Their dissipated energy is about 1.21 J for  $T_{CASE} = 25^\circ\text{C}$  and 1.10 J for  $T_{CASE} = 150^\circ\text{C}$ . The dissipated energy the device can sustain decreases by 10% when ambient temperature is varying from  $25^\circ\text{C}$  to  $150^\circ\text{C}$ .

Another set of tests on C-MOSFETs are performed with gate driver resistor  $R_G = 47 \Omega$ . In Fig. 10, first failures of gate oxide show up simultaneously at 21  $\mu$ s with dissipated energy of 1.58 J and 1.46 J for  $T_{CASE} = 25^\circ\text{C}$  and  $150^\circ\text{C}$  respectively. Second failure is due to thermal runaway caused by heat generation after first oxide failure. So, the failure between gate and source is viewed as the main failure factor for these tests.

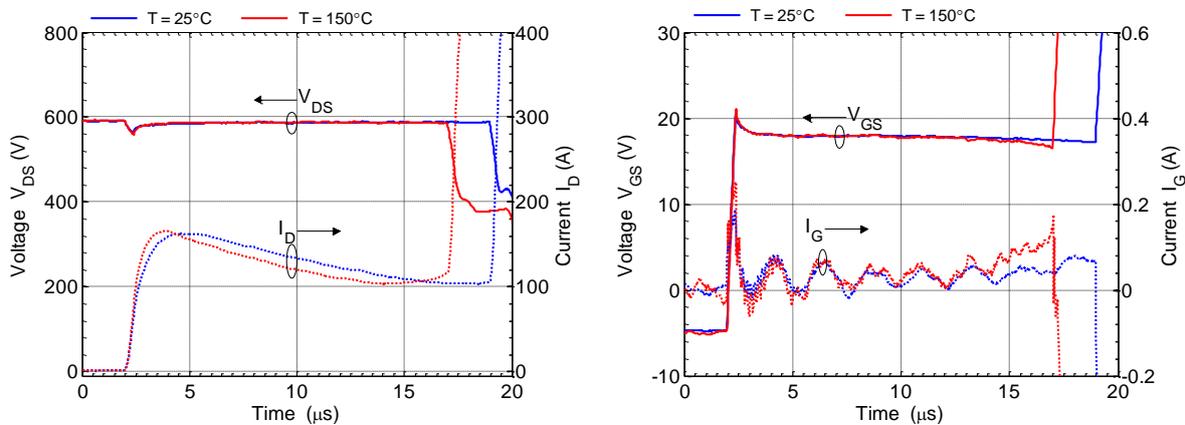


Fig. 9. Failure of A-MOSFET: drain and gate waveforms, for  $R_G = 10 \Omega$ ,  $T_{CASE} = 25^\circ\text{C}$  and  $150^\circ\text{C}$ .

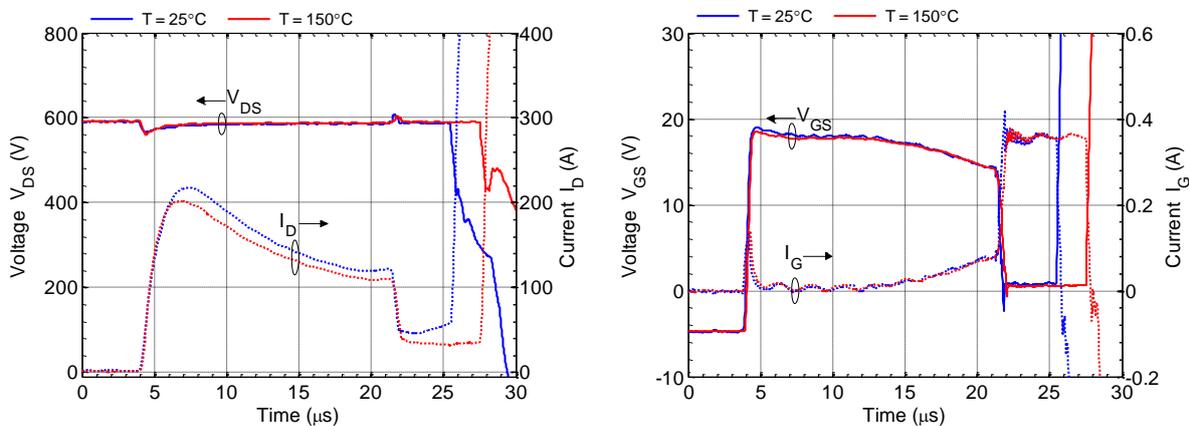


Fig. 10. Failure of C-MOSFET: drain and gate waveforms, for  $R_G = 47 \Omega$  at  $T_{CASE} = 25^\circ\text{C}$  and  $150^\circ\text{C}$ .

According to these experiments, results show that maximum dissipated energy is relevant to the initial case temperature. Experimental and numerical results presented in [5] and [11] propose that even if the initial case temperatures are different, the increase of the die metallization temperature beyond a critical value (e.g. fusion temperature of aluminium metallisation of 900 K), is responsible to device failure.

### 5.2. Effect of gate resistance

Significant gate leakage current appearing during SC that results in the decrease in the gate voltage as mentioned above. It seems that increase in the gate leakage current is

responsible for the device failure. If so, can the solution of limiting gate leakage current by a larger gate driver resistor improve MOSFET's short circuit withstand capability? A validation test is carried out with two different gate resistors on B-MOSFET and C-MOSFET.

B-MOSFET was tested for bus voltage = +600 V and driver voltage = +18 V at  $T_{CASE} = 150^{\circ}\text{C}$ . We have noticed lower gate leakage current and less oscillation in the case of gate driver resistor = 47  $\Omega$  (Fig. 11 (b)). Their failures comes almost at the same moment and dissipated energy is estimated about 669 mJ and 660 mJ for  $R_G = 10 \Omega$  and  $R_G = 47 \Omega$  respectively even if the maximum gate leakage current is significantly reduced when  $R_G = 47 \Omega$ .

Fig. 12 reports waveforms of C-MOSFET measured at ambient temperature  $T_{CASE} = 25^{\circ}\text{C}$ . First failure appearing simultaneously, C-MOSFET is capable to sustain dissipated energy about 1.61 J for  $R_G = 10 \Omega$  and 1.59 J for  $R_G = 47 \Omega$ .

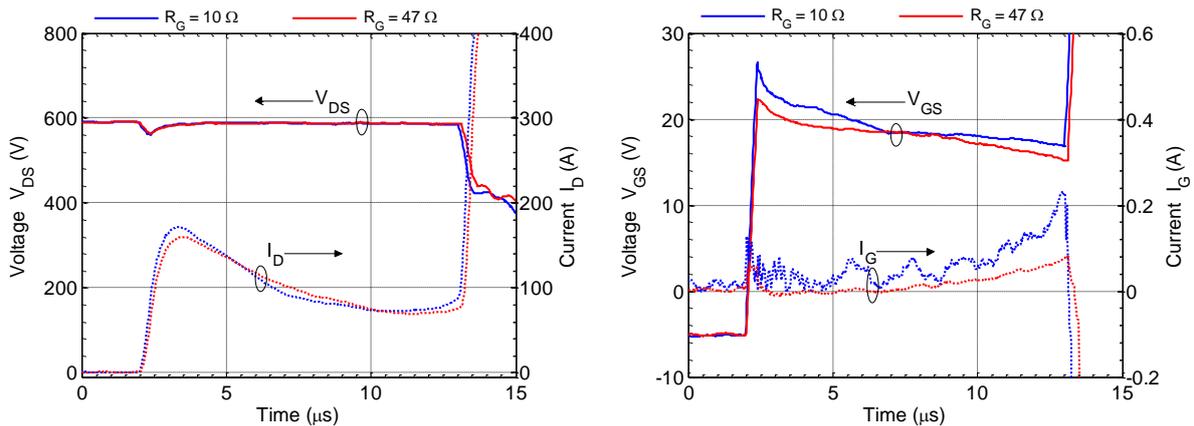


Fig. 11. Failure of B-MOSFET: drain and gate waveforms, at  $T_{CASE} = 150^{\circ}\text{C}$  for  $R_G = 10 \Omega$  and 47 $\Omega$ .

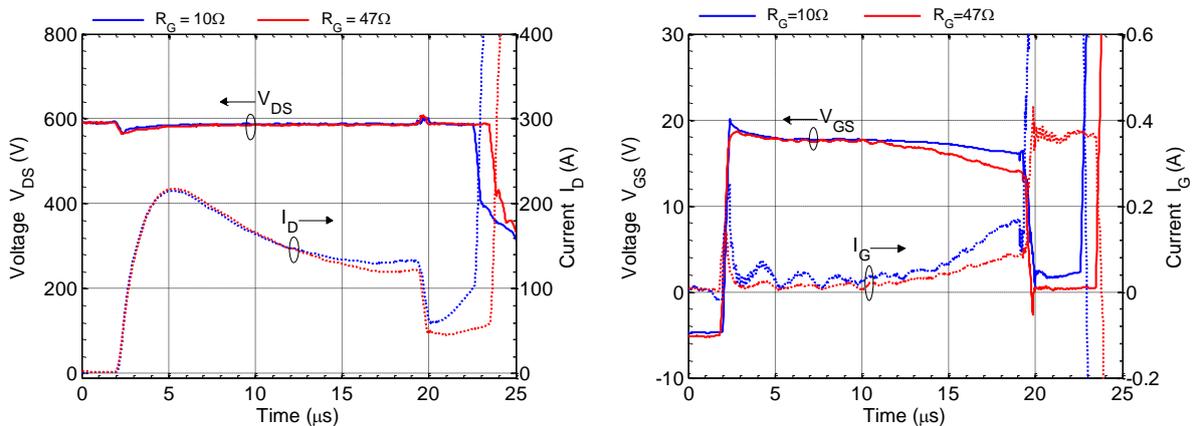


Fig. 12. Failure of C-MOSFET: drain and gate waveforms, at  $T_{CASE} = 25^{\circ}\text{C}$  for  $R_G = 10 \Omega$  and 47 $\Omega$ .

As dissipated energies until failure are much closed, we have not seen any proof of improving robustness by increasing gate resistance values. The disparity in behavior, inherent to the transistors of a same lot, do not allow us to conclude that the gate resistance has no effect on the robustness of the SiC MOSFET, nevertheless, the above results refute our hypothesis and demonstrate that it is not possible to improve robustness in short circuit operation by limiting gate leakage current. These results tend also to show that the tunneling current appearing during SC is not necessary responsible for the device failure. Another mode of failure can be considered like fusion of the source metallization as mentioned in [11].

## 6. Conclusions

This paper deals with the robustness of SiC MOSFET in short circuit operation. First section focuses on characteristic of SiC MOSFET under current limitation. Mechanism of failure is found out through single shoot destructive test. Failure is caused by short-circuit between gate and source or between drain and source that seems to be related to thermal runaway.

For A and B MOSFETs, failure between gate and source appears simultaneously with the failure between drain and source. The destruction of these devices under current limitation firstly appears in an on-state. For C-MOSFETs, failure between gate and source precedes destruction between drain and source. The failure with a short-circuit between gate and source controls in a first step the drain current, but, due to the high level of the leakage drain current, failure between drain and source seems to appear after thermal runaway.

Critical energy estimation is realized by successive tests with increased SC duration. In these conditions delayed failure of A-MOSFET appears few  $\mu\text{s}$  after applying the negative gate voltage (-5V). Behavior of C-MOSFET is completely different. We observe after turn off of drain current by applying a negative voltage on the gate a failure between gate and source appearing few  $\mu\text{s}$  after drain current switch-off. The short circuit between gate and source maintain the component in an off state. This particular behavior, if reproducible, could be very interesting for safety or reconfiguration aspects of power electronics converters.

The paper also shows that ambient temperature has a significant effect on the robustness of SiC MOSFETs. This point tends to show that failures (of the oxide, between gate and source or between drain and source) are related to temperature increase during short-circuit. We have also shown that increasing the gate resistance and reducing the tunneling gate current seems to have no influence on the robustness. This tends to show that the failure of the oxide or between gate and source seems to be not correlated with the tunneling current but mainly to the temperature inside the device.

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